CMI Low Power Implementation

Overview: CMI Low Power Architecture is based on Ace Low power spec V2, with always Autowake enable mode, Where CMI Master Bridge will generate the Autowake signal (mapped to QActive signal of Qchannel interface) depending, by resolving the dependencies of slaves, it is connected to. And also Issue Qdeny whenever an autowake event occurs prior to having issued fence\_ack\_n.

The transactions pending to a particular slave is tracked with respect to their Power Target, which is mapping of group of Slave Bridges. Tracking is done based on count of all pending responses to the Power Target.

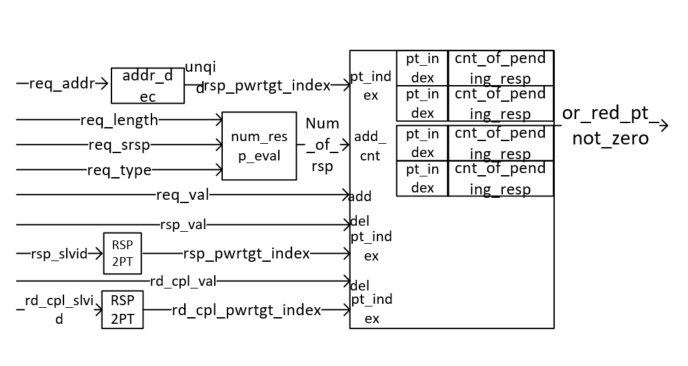
1. CMI bridges have no clock & power domain crossing
   1. This means no VDC.
   2. Clock & power boundaries are between router<->router and/or router<->bridge only.  Not within the bridge or between bridge & host.
2. The CMI NoC itself can have power domain crossing(router <-> router and/or router<->bridge).
   1. CMI master bridge still needs to support low power to wake up the power domains along the routes.
   2. Low power verification still applies here for the NoC.
3. CMI low power is autowake-only because CMI protocol has no decode error.
   1. Note that this restriction is CMI only and has **NOT** been confirmed for IDI NoCs yet.

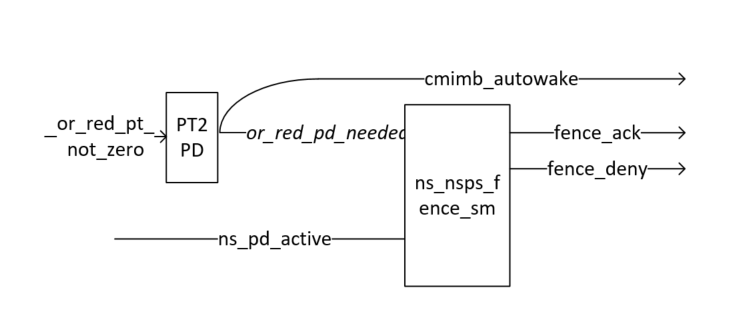
Implementation Details:

CMI Master Bridge Low Power Interface Signals:

|  |  |  |  |
| --- | --- | --- | --- |
| Direction | width | Signal Name | Description |
| i/p | [P\_NUM\_PD-1:0] | nsps\_pd\_active; | Indicates whether targets within the power domain are active and reachable. Indicates power domain is either turned off, or in the process of being turned off. Point to multi-point, subject to clock/voltage domain crossing treatment. |
| o/p | [P\_NUM\_PD-1:0] | cmimb\_fence\_ack\_n; | Signal indicating pd\_active\_<PD> 1->0 transition has been observed and fencing has begun. Should remain asserted until 0->1 transition on pd\_active\_<PD>. Point to point, subject to combinatorial aggregation to create fence\_ack\_asserted\_<PD>\_n with all such signals targeting the same power domain. |
| o/p | [P\_NUM\_PD-1:0] | cmimb\_fence\_deny; | whenever an autowake event occurs prior to having issued fence\_ack\_n, fence\_deny will be asserted |
| o/p | [P\_NUM\_PD-1:0] | cmimb\_autowake; | Request to restore power in response to new transactions on host interface attempting to reach target within power domain. Point to point, subject to combinatorial aggregation with all wake signals targeting the same power domain. |
| i/p |  | nsps\_sleep\_req\_n; | Inform NS logic of intent to remove power from power domain <PD>. Point to multi-point, subject to clock/voltage domain crossing treatment. |
| o/p |  | cmimb\_sleep\_ack\_n; | Response to sleep\_req\_<PD>\_n, indicates NoC logic is in state safe for power removal. Point to point, subject to combinatorial aggregation with like signals originating from the same power domain. |
|  |  |  |  |
| Param |  | P\_NUM\_PD | Number of Power Domains |
| Param |  | P\_PT\_NUM | Number of PowerTargets |
| Param |  | P\_PTID\_WIDTH | PowerTarget Width, in one hot mapping equal to P\_PT\_NUM. |
| Param |  | P\_NUM\_SLAVEID | Number of Slaves with traffic configured through this master bridge |
| Param |  | P\_SLVID\_WIDTH | Bridge Id of the slave module. 16 bits |
| Param | [(P\_NUM\_SLAVEID\*(P\_SLVID\_WIDTH+P\_PTID\_WIDTH))-1:0] | P\_SLVID\_RESP\_PT\_LIST | Table to lookup the Power Target from the Response SlaveID |
| Param | [(P\_PT\_NUM\*(P\_PTID\_WIDTH+P\_NUM\_PD)-1:0] | P\_PT\_ACTIVE\_PD\_LIST | Table to lookup the Active(Grouped)PowerDomains from the Power Target |
| param |  | P\_LP\_EN | Low Power Enable |

Following is the block diagram of the implementation.





Details of Components:

Address Decoder: The Address Decoder will provide the Power Target Information corresponding to every request. The unqid Field will be used for the Power Target Value and it’s Width P\_UNQID\_WIDTH will be mapped to P\_PTID\_WIDTH programmed from the NocStudioo.

Num\_resp\_eval: Based on the type of request, this module will compute the number of responses based on whether the transaction is read or write transaction, and calculate the number of read completion beats based on bus width configured, 32B or 64B, and whether a response is expected based on rd\_srsp signal value. For writes it will be fixed.

Power Target Counter Tracker: For every CMI request, once Power Target corresponding to that request is decoded and Num of responses are evaluated, in the Power Target tracker the counter belonging to the Power Target Index decoded by the address decoder will be incremented by the value evaluated Num\_resp\_eval module and based on the responses and read completions received during the transaction they will get decremented. Once a counter of a Power Target has Zero Value, The Corresponding Power Domains Autowake signal which is mapped to the Qactive signal to the PMU can be safely deasserted. And as the counter value for a Power Target increments to a nonzero value the Autowake signal is asserted to intimate the PMU through Qactive signal and also sends fence deny if the device has received any power down request.

RSP2PT: The transactions from each slave will now carry slavid information in the packet and slavid will translated to Power Target information based on Parameter Listing programmed by the Noc Studio.

PT2PD: One more parameter listing is required to translate the Power Target Information their respective Power Domains.

Ns\_nsps\_fence\_sm: This module is reused from the Ace LP implementation. This module employs the handshake with the Power Supervisor module for each power up and power down requests. In case of autowake event during the power down, this module will issue fence\_deny which will be translated to Qdeny handshake to the PMU.

References:

1. low-power-spec-v2.docx
2. Coherency Power Management
3. [Staged Fencing and Autowake](https://netspeed.atlassian.net/wiki/spaces/EN/pages/10911749/Staged+Fencing+and+Autowake)